

REMARKS

Response to §112 Rejection of Claim 20

In the June 29, 2005 Office Action, the Examiner rejected claim 20 under 35 U.S.C. §112, first paragraph for alleged non-compliance with the written description requirement. Specifically, the Examiner asserted that the limitation "a silicon nitride oxide layer located on at least said gate stack" as recited by claim 20 is not described in the specification and shown in the drawings.

Applicants respectfully disagree with the Examiner's assertion and hereby direct the Examiner's attention to Figure 6 and paragraph [0031] of the instant specification as originally filed. Figure 6 shows a thin silicon nitride (SiN) etchstop layer located over the entire MOSFET including the gate stack, which is therefore "located on at least the gate stack" as recited by claim 20. Further, Figure 6 and paragraph [0031] of the instant specification describe ISSG oxidation of the thin silicon nitride (SiN) etchstop layer so as to form oxide, i.e., nitridized silicon oxide or silicon nitride oxide.

It is therefore clear that the instant specification as originally filed describes a thin silicon nitride oxide layer, which is formed by an ISSG oxidation process and is located on at least the gate stack. Applicants correspondingly request the Examiner to withdrawn the §112 written description rejection of claim 20.

Response to §103 Rejection of Claim 16-18 and 20

The Examiner rejected claims 16-18 and 20 under 35 U.S.C. §103(a) for alleged obvious over U.S. Patent No. 6,482,726 to Aminpur et al. (hereinafter "Aminpur") in view of U.S. Patent No. 6,639,264 to Loh (hereinafter "Loh").

Applicants respectfully traverse the Examiner's obviousness rejection, for the following reasons.

35 U.S.C. §103(c) expressly provides that:

“Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.”

The Loh patent was issued on October 28, 2003 on the basis of U.S. Patent Application No. 09/210,247 filed on December 11, 1998. Further, the Loh patent was assigned to International Business Machines Corporation (“IBM”) on December 11, 1998 (see the Assignment Recordation at Reel No. 009645 and Frame No. 0452) and has been owned by IBM since then.

The present application is a divisional of U.S. Patent Application No. 10/345,344 filed on January 15, 2003, which was assigned to IBM on January 15, 2003 (see the Assignment Recordation at Reel No. 013689 and Frame No. 0676) and has been owned by IBM since then.

Since the Loh patent is a patent that was not issued until after the priority date of the present application and falls under subsection (e) of 35 U.S.C. §102, and since the subject matter of the Loh patent and the claimed invention of the present application were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person, the Loh patent cannot be used against the claimed invention of the present application in light of 35 U.S.C. §103(c).

Further, the Examiner has expressly conceded in the June 29, 2005 Office Action that the primary reference Aminpul fails to disclose fluorine doped low K dielectric oxide gate spacers with a fluorine content of about $1\text{E}14$ to $1\text{E}16 \text{ cm}^{-2}$ (see the Office Action, page 3, 14-15), as positively recited by claim 16 of the present application, from which claims 17-18 and 20 depend, but attempted to remedy such deficiency of Aminpul by citing the Loh patent.

In light of the above-explained removal of the Loh patent from prior art, it is clear that the Aminpul patent alone does not teach or suggest the claimed invention of the present application.

Therefore, Applicants respectfully request the Examiner to reconsider, and upon reconsideration to withdraw, the §103 rejections of claims 16-18 and 20.

New Claim 21

New claim 21 has been added herein, which recites a MOSFET device that comprises a silicon substrate having shallow trench isolation STI located therein, a gate dielectric and a gate stack located on the silicon substrate, a fluorine doped low K dielectric oxide gate spacer located on sidewalls of the gate stack, and a silicon nitride oxide layer located on at least the gate stack.

In the June 29, 2005 Office Action, the Examiner expressly conceded that Aminpul fails to disclose any silicon nitride layer formed over the MOSFET (see the Office Action, page 5, lines 4-5), much less a silicon nitride oxide layer located on at least the gate stack, but attempted to remedy such deficiency of Aminpul by citing the Loh patent.

In light of the above-explained removal of the Loh patent from prior art, it is clear that the Aminpul patent alone does not teach or suggest any silicon nitride layer formed over the MOSFET, much less a silicon nitride oxide layer located on at least the gate stack.

Therefore, the newly added claim 21 patentably distinguishes over Aminpul by positively reciting a silicon nitride oxide layer located on at least the gate stack.

The addition of new claim 21 herein does not increase the number of total claims beyond the number for which payment was previously made. Therefore, no fee is rendered payable for this Response.

CONCLUSION

Based on the foregoing, claims 16-18 and 20-21, now pending in the application, are in condition for allowance. Issue of a Notice of Allowance for the application is therefore requested.

If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,



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